## ABSTRACT OF THE DISCLOSURE

Disclosed is an integrated circuit that includes clock generation circuitry which generates a master clock signal and at least one other clock signal. The master clock signal and the other clock signal are transmitted through a clock distribution tree to a circuit component. In a default mode, the circuit component receives the master clock signal at a first component block to create a first time domain for the first component block and receives the other clock signal at a second component block to create a second time domain for the second component block. Bypass logic creates a bypass path to allow the second component block to receive the master clock signal such that the clock domain of the second component block is the same as the clock domain of the first component block such that signals can be transferred between the clock domains with reduced latency.